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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,418	08/24/2001	Daniel J. Dove	10015055-1	4205

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EXAMINER	
KHUONG, LEE T	
ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,418	DOVE, DANIEL J.	
	Examiner	Art Unit	
	Lee Khuong	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-8 and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Lo (US 6,920,132).

Regarding claims 1, 8 and 13, Lo teaches an apparatus and a method for Reduced Pin Gigabit Media Independent Interface. Lo's apparatus and method comprising: an interfacing a media access controller (MAC) (22, Fig. 1, ***MAC***) and a physical layer device (PHY) (26, Fig. 1, ***PHY***) in a manner whereby the standards of IEEE 802 are complied with for at least one of the gigabit media independent interface (see col. 1, lines 28-40, col. 2, lines 11-17, col. 4, line 50 – col. 5, line 4) and the ten bit interface (see col. 7, line 51 – col. 8, line 25, col. 9, lines 12-28 and col. 10, line 44 – col. 11, line 25, ***the preamble of a data packet is an initial eight bit sequence with one bit for the rising edge of the receiving clock and one additional bit for the falling edge of the receiving clock***), transferring data at a predetermined rate while substantially reducing the required number of input and output pins (Fig. 5, see col. 9, lines 12-28 and col. 11, lines 30-47), said apparatus comprising: means for multiplexing the data and control signals that are normally applied to a predetermined number of pins to a significantly lesser number of pins

and for selectively mapping the data and control signals to the lesser number of pins (see col. 1, line 28 – col. 2, line 27 and col. 11, lines 30-47).

Regarding claim 2, Lo teaches all limitations set forth in the rejection of claim 1. Lo further teaches wherein said multiplexing means multiplexes different significant bits of data on the same set of pins using both edges of a clock signal having the predetermined rate, thereby transferring data at the predetermined rate on the lesser number of pins (Fig. 5, see col. 7, line 51 – col. 8, line 65, col. 9, lines 12-28 and col. 10, line 44 – col. 11, line 25).

Regarding claim 3, Lo teaches all limitations set forth in the rejection of claim 1. Lo further teaches wherein the clock rate is within the range of about 2.5 MHz and about 125 MHz, with the clock rate being within the range of about 2.5 and about 25 MHz for the ten bit interface and about 125 MHz for the gigabit media independent interface operation (see col. 12, lines 60-61).

Regarding claim 5, Apparatus as defined in claim 3 wherein the clock signal has a duty cycle for gigabit media independent interface operation that is within the range of 45 and 55 percent and a duty cycle for the ten bit interface operation that is within the range of 40 and 60 percent.

Regarding claims 6 and 10, Lo teaches all limitations set forth in the rejection of claims 1 and 8. Lo further teaches comprising six input pins (42, 44 and 46 of Fig. 3) for use in either

the gigabit media independent interface operation or the ten bit interface operation in which: a transmit reference clock signal TXC (44, Fig. 3) is applied to a first pin in the gigabit media independent interface operation and the ten bit interface operation (see col. 5, line 45 – col. 8, line 56); 8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation (see col. 7, line 51 – col. 8, line 25, col. 9, lines 12-28 and col. 10, line 44 – col. 11, line 25); 2 bits of data are applied to the sixth pin in the ten bit interface operation (see col. 7, line 51 – col. 8, line 25, col. 9, lines 12-28 and col. 10, line 44 – col. 11, line 25); and, control signals are applied to the second through fifth pin in the gigabit media independent interface operation (see col. 5, line 45 – col. 8, line 56).

Regarding claims 7 and 11, Lo teaches all limitations set forth in the rejection of claims 1 and 8. Lo further teaches comprising six output pins (62, 64 and 66 of Fig. 3) for use in either the gigabit media independent interface operation or the ten bit interface operation in which: a receive reference clock signal RXC (64, Fig. 3) is derived from the received data stream and appears on a first pin in the gigabit media independent interface operation and the ten bit interface operation (see col. 5, line 45 – col. 8, line 56); 8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation (see col. 7, line 51 – col. 8, line 25, col. 9, lines 12-28 and col. 10, line 44 – col. 11, line 25); 2 bits of data are applied to the sixth pin in the ten bit interface operation (see col. 7, line 51 – col. 8, line 25, col. 9, lines 12-28 and col. 10, line 44 –

col. 11, line 25); and, control signals are applied to the second through fifth pin in the gigabit media independent interface operation (see col. 5, line 45 – col. 8, line 56).

Regarding claim 12, Lo teaches all limitations set forth in the rejection of claim 8. Lo further teaches wherein CRS and COL signals are applied on the same pin (see col. 6, lines 5-9 and col. 8, lines 27-28).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo.

Regarding claim 4, Lo teaches all limitations set forth in the rejection of claim 1. Lo further teaches wherein said multiplexing means includes means for controlling the relative timing between the clock signal and the data during transmitting and during receiving, the clock and data signals being generated substantially simultaneously when either the MAC or the PHY transmits the signals (Fig. 5, see col. 7, line 51 – col. 8, line 65, col. 9, lines 12-28 and col. 10, line 44 – col. 11, line 25), such that the data to clock output skew at the transmitter is within +/- 500 picoseconds (this range is a well known feature when transmitting a signal with controlling the jittering in a signal as evidenced by {**Gillespie et al.** (US 6,215,816), col. 37, line 66 – col.

38, line 9, ***a few hundred picoseconds***}) and the data to clock input skew at the receiver is between about 1 and about 2.8 nanoseconds for clock signal speeds within the range of 2.5 MHz and 125 MHz (this range is a well known feature when receiving a signal with the delay from one source to the next between the ranges of around 1 nanosecond as evidenced by {**Gillespie et al.** (US 6,215,816), col. 39, lines 30-38}).

Lo does not expressly teach the jitter of the transmitting signal in a specific +/-500 picoseconds and the delay of the receiving signal in the range between 1 and about 2.8 nanoseconds.

However, it also would have been obvious to a person of ordinary skill in the art to choose the ranges specified by the applicant as a design choice.

Regarding claim 9, Lo teaches all limitations set forth in the rejection of claim 8. Lo does not expressly teach the reduced number of pins is 12.

Lo does teach the TXD [3:0] and the RXD [3:0] in Fig. 3 can be easily recognized to be equivalent with the eight pins of the applicant TXD 0 – 3 and RXD 0-3.

As a design choice at the time of the invention, it would have been obvious to a person of ordinary skill in the art to split Lo's TXD and RXD to the applicant's TXD and RXD.

Response to Arguments

5. Applicant's arguments filed on 6/30/2005 have been fully considered but they are not persuasive. Regarding applicant's argument on page 7, lines 7-10, and the disclosure of the Affidavit filed on 6/30/2005 that dated on 9/22/2000, page 7 of 14, line 3 and the original claim

9, all stated the RGMII has 12 pins, which is contradicting the applicant stated that it should have 13 pins. Examiner respectfully requesting the applicant to please clarify the specification or the drawing is correct and correct accordingly to be persistent with each other.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Juszkiewicz et al. (US 6,353,169) is cited to show a jitter range of a transmitting signal is designed within a +/-500 picoseconds.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lee Khuong whose telephone number is 571-272-3157. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lee T. Khuong
Examiner
Art Unit 2665

ALPUS H. HSU
PRIMARY EXAMINER